a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming a first ion implanted layer of the second conductivity, at least upper part of which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of the first conductivity type; and

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and the pocket dopant diffused layer of the second conductivity type, which is in contact with a bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively,

wherein the pocket dopant diffused layer includes, in a portion in contact with the extended high-concentration dopant diffused layer, a segregated part that has been formed through segregation of the heavy ions.

Please add new claims 20-24 as follows:

--20. A method for fabricating a semiconductor device according to claim 6, wherein the second step of implanting heavy ions is performed at an implant energy such that the range of the heavy ions implantation is within the second ion implanted layer formed in the third step.

21. A method for fabricating a semiconductor device according to claim 6, wherein the first dopant is arsenic.

22. A method for fabricating a semiconductor device according to claim 21, wherein the heavy ions are indium ions.

23. A method for fabricating a semiconductor device according to claim 8, wherein the heavy ions are indium ions, and the first dopant and the second dopant are arsenic.